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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,779	03/18/2004	Hirofumi Harada	S004-5242	8062

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EXAMINER
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DOAN, THERESA T

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/803,779

Applicant(s)

HARADA, HIROFUMI

Examiner

Theresa T. Doan

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 August 2006.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1.3-5 and 7-24 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1.3-5 and 7-24 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☒ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. The amendment filed on 08/21/06 is acknowledged. By this amendment, claims 1, 3-5, and 7-24 are pending in this application.

#### *Claim Objections*

2. Claims 3-5 and 8-12 are objected to because of the following informalities:

In claim 3, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 3, line 2, ";" after "claim 1" should be changed to -- , --.

In claim 4, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 4, line 2, ";" after "claim 3" should be changed to -- , --.

In claim 5, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 5, line 2, ";" after "claim 1" should be changed to -- , --.

In claim 8, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 8, line 2, ";" after "claim 7" should be changed to -- , --.

In claim 9, line 1, "A vertical" should be changed to - - The vertical - -.

In claim 9, line 2, ";" after "claim 8" should be changed to -- , --.

In claim 10, line 1, "A vertical" should be changed to -- The vertical --.

In claim 10, line 2, ";" after "claim 7" should be changed to --, --.

In claim 11, line 1, "A vertical" should be changed to -- The vertical --.

In claim 11, line 2, ";" after "claim 7" should be changed to --, --.

In claim 12, line 1, "A vertical" should be changed to -- The vertical --.

In claim 12, line 2, ";" after "claim 7" should be changed to --, --.

Similarly, in the new claims 13-20 and 22-24, the use of the article "A" to preface the preamble of the dependent claims should be changed to "The", and the use of a semicolon to separate the preamble from the body of the dependent claims should be changed to comma.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2814

4. Claims 1, 3-5 and 7-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon et al. (U.S. Pat. 6,351,009) in view of Yamada et al. (U.S. Pub. 2001/0025973).

Regarding claims 1, 3, 7-11, 16, 20-21 and 23, Kocon (Fig. 2D) discloses a vertical MOS transistor comprising: a semiconductor substrate 201 of a first conductivity type (N+); an epitaxial growth layer 203 (column 3, lines 46-51) of the first conductivity type (N) which is formed on the semiconductor substrate 201; a body region 205 of a second conductivity type (P) which is formed on the epitaxial growth layer 203; a heavily doped body contact region 204 of the second conductivity type (P+) formed on a part of a surface of the body region 205; a heavily doped source region 206 of the first conductivity type (N+) formed on a part of the surface of the body region 205 that is not covered with the heavily doped body contact region 204; a silicon trench 207 piercing the body region 205 and the heavily doped source region 214 to reach an inner part of the epitaxial growth layer 203; a gate insulating film 208 formed along side wall surfaces and bottom surfaces of the silicon trench; a heavily doped polycrystalline silicon gate 210 (column 3, lines 57-62) buried in the silicon trench 207 over the gate insulating film 208 to a level of the heavily doped source region 206 (column 3, lines 26-28); an intermediate insulating film 212 formed on the heavily doped polycrystalline silicon gate 210 in the silicon trench 207 to reach a surface the semiconductor substrate; a metallic source electrode 215 (column 4, lines 16-19) having a flat surface in contact with the intermediate insulating film 212, the heavily doped source region 206, and the heavily

doped body contact region 204; and a metallic drain electrode (not shown, see column 4, lines 19-21) connected to a rear surface of the semiconductor substrate 201.

Kocon does not disclose side spacers disposed on the sidewalls of the silicon trench and above the gate.

However, Yamada (Fig. 42) teaches a MOS transistor having an intermediate insulating film 42a formed on the gate 9 in the trench, and the side spacers 41 of silicon nitride (par. [0154], lines 1-8) disposed on the sidewalls of the trench and above the gate 9. Accordingly, it would have been obvious to modify the MOS transistor of Kocon by forming the side spacers of silicon nitride on the sidewalls of the trench and above the gate because such forming of those side walls would control or prevent the peeling of the gate insulating film, as taught by Yamada (par. [0154], lines 1-10).

Regarding claims 4-5 and 12, Kocon further discloses that the gate 210 is buried within gate trench to permit the inclusion of dielectric layer 212 of sufficient thickness to provide gate isolation (column 3, lines 36-40). And the sufficient thickness of the dielectric layer for providing gate isolation is about 0.5  $\mu\text{m}$  to 0.8  $\mu\text{m}$  (column 1, lines 63-67 through column 2, lines 1-4). Accordingly, it would have been obvious to form the gate 210 buried 0.5  $\mu\text{m}$  to 0.8  $\mu\text{m}$  down from a top of the silicon trench 207 in order to permit the inclusion of the dielectric layer 212 of sufficient thickness to provide gate isolation. It is noted that it has been held that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235

Art Unit: 2814

(CCPA 1955). In this case, there is no evidence of the criticality of the claimed range, the claimed range will not support the patentability of subject matter encompassed by the prior art.

Regarding claims 13-14 and 17-18, Yamada (Fig. 42) further teaches that the intermediate insulating film 42a is formed directly on the gate 9 and the side spacers 41, and the side spacers 41 are disposed between the gate insulating film 8 and the intermediate insulating film 42a.

Regarding claims 15, 19, 22 and 24, Kocon teaches the intermediate insulating film 212 made of silicon dioxide (column 3, lines 63-65) to provide gate isolation (column 3, lines 36-38). And Yamada teaches the side spacers 41 made of silicon nitride (par. [0154], lines 1-8) and the intermediate insulating film 42a made of silicon nitride (par. [0154], lines 10-16) to provide gate isolation (par. [0154], lines 20-25). Accordingly, it would have been obvious to form the intermediate insulating film with silicon nitride, which is the same material as side spacers, or with silicon dioxide, which is different material from side spacers because both silicon dioxide and silicon nitride are equivalent materials in using to provide gate isolation.

### ***Response to Arguments***

5. In response to Applicant's arguments regarding the claim rejections, the new reference is applied in the new ground of rejection.

6. Regarding claim objections, Applicant argues that the use of the phrase "A vertical MOS transistor" instead of "The vertical MOS transistor" to preface the preamble of the dependent claims and the use of a semicolon instead of a comma to separate the preamble from the body of the dependent claims are standard and widely accepted claim drafting techniques.

It is noted that the element "A vertical MOS transistor" recites in the preamble of the dependent claims is not a first mentioned, it was mentioned earlier in the independent claims. Therefore, the element "A vertical MOS transistor" recited in the preamble of the dependent claims should be changed to "The vertical MOS transistor" according to M.P.E.P §2173.05 (e). It is further noted that the use of a semicolon instead of a comma to separate the preamble from the body of the dependent claims seems to be a grammatical error.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the



Art Unit: 2814

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Theresa Doan  
October 27, 2006.